WHAT IS CLAIMED IS:

1. A method of manufacturing a memory integrated circuit device including a memory cell region and a peripheral circuit region on a semiconductor substrate, the method comprising the steps of:

(a) forming a first groove in the memory cell region on the semiconductor substrate;

(b) forming a second groove in the peripheral circuit region on the semiconductor substrate; and

(c) forming a memory cell transistor in self-alignment with the first groove in the memory cell region and forming a peripheral circuit transistor in the peripheral circuit region using the second groove as an isolation groove,

wherein said steps (a) and (b) are performed simultaneously.

2. The method as claimed in claim 1, wherein said steps (a) and (b) are performed using a single mask.

3. The method as claimed in claim 1, further comprising the step of (d) increasing a depth of the second groove with respect to a depth of the first groove.

4. The method as claimed in claim 1, wherein said step (c) comprises the steps of:

(d) filling the second groove with an isolation insulating pattern in the peripheral circuit region;

(e) forming a first insulating film on a surface of the semiconductor substrate so that the first insulating film successively covers the surface of the semiconductor substrate and a surface of the first groove in the memory cell region;

(f) removing the first insulating film from the surface of the semiconductor substrate except for the memory cell region;

(g) forming a second insulating film on the surface of the semiconductor substrate in the peripheral circuit region; and

(h) forming a conductive film on the semiconductor substrate so that the conductive film covers the first insulating film in the memory cell region and the second insulating film in the peripheral circuit region.

5. The method as claimed in claim 4, further comprising the step of (i) forming a first gate electrode in the memory cell region and a second gate electrode in the peripheral circuit region by performing patterning on the conductive film in the memory cell region and the peripheral circuit region using a single mask.

6. The method as claimed in claim 4,

further comprising the step of (j) forming a thermal oxide film on a surface of the second groove before said step (d).

7. The method as claimed in claim 4, wherein:

the first insulating film includes a nitride film and forms an electric charge storing layer; and

the conductive film is formed in contact with the first insulating film.

8. The method as claimed in claim 4, further comprising the step of (i) forming a conductive diffusion region of a first conduction type on the surface of the semiconductor substrate except for the first groove in the memory cell region and except for the peripheral circuit region before said step (e) after said step (d).

9. The method as claimed in claim 8, wherein:

said steps (a) and (b) comprise the steps of:

(j) forming a mask layer on the semiconductor substrate and forming openings corresponding to the first and second grooves in the mask layer; and

(k) forming the first and second grooves corresponding to the openings by etching the semiconductor substrate using the mask layer as a mask;

said step (d) comprises the steps of:

(l) depositing an isolation insulating film on the mask layer so that the isolation insulating film fills the first and second grooves, and polishing and removing the isolation insulating film deposited on the mask layer using the mask layer as a stopper; and

(m) removing the mask layer; and

said step (i) is performed by performing ion implantation of an impurity element of the first conduction type using film patterns of the isolation insulating film as a self-alignment mask, the film patterns remaining in the first and second grooves.

10. The method as claimed in claim 9, further comprising the step of (n) forming a conductive diffusion region of a second conduction type at the bottom of the first groove in the semiconductor substrate in the memory cell region.

11. The method as claimed in claim 4, further comprising the step of (i) selectively forming a conductive diffusion region of a first conduction type on a bottom face of the first groove after said step (d) before said step (e).

12. The method as claimed in claim 11, further comprising the step of (j) selectively forming a conductive diffusion region of a second conduction type on the bottom face of the first groove after said step (d) before said step (i).

13. The method as claimed in claim 12, wherein:

said steps (a) and (b) comprise the steps of:

(k) forming a mask layer on the semiconductor substrate and forming openings corresponding to the first and second grooves in the mask layer; and

(l) forming the first and second grooves corresponding to the openings by etching the semiconductor substrate using the mask layer as a mask;

said step (d) comprises the steps of:

(m) depositing an isolation insulating film on the mask layer so that the isolation insulating film fills the first and second grooves, and polishing and removing the isolation insulating film deposited on the mask layer using the mask layer as a stopper; and

(n) removing the isolation insulating film from the first groove; and

said step (i) is performed by performing ion implantation of an impurity element of the first conduction type using the mask layer as a self-alignment mask.

14. The method as claimed in claim 12, wherein said step (j) comprises the step of (k) performing ion implantation of an impurity element of the second conduction type at an angle on a sidewall face of the first groove.

15. The method as claimed in claim 14, further comprising the step of (l) performing ion implantation of an impurity element of the first conduction type at an angle on the sidewall face of the first groove after said step (k).

16. The method as claimed in claim 4, further comprising the steps of:

(i) depositing an additional conductive film so that the additional conductive film covers the first insulating film;

(j) forming a sidewall insulating film on a sidewall face of the first groove as a floating gate electrode by etching back the additional conductive film, the sidewall insulating film being formed of the additional conductive film; and

(k) depositing an additional insulating film so that the additional insulating film covers the sidewall insulating film,

wherein:

said steps (i), (j), and (k) are performed before said step (h) after said step (e); and

the conductive film is formed in contact with the additional insulating film.

17. The method as claimed in claim 1, wherein the semiconductor substrate further includes a pumping circuit region, the method further comprising the steps of:

(d) forming a third groove in the pumping circuit region on the semiconductor substrate simultaneously with said steps (a) and (b) using a single mask; and

(e) forming a pumping capacitor in the third groove in the pumping circuit region.